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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
AUDUONG, GENE NGHIA	
ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 04/24/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No	Applicant(s)	
	10/042,604	HSU, LOUIS ET AL.	
	Examiner	Art Unit	
	Gene N Auduong	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is FINAL. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-24 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-11 and 17-24 is/are rejected.

7)☒ Claim(s) 12-16 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. Claims 1-11 and 17-24 are rejected under 35 U.S.C. 102(a) as being anticipated by Ishikawa (U.S. Pat. No. 6,314,048).

Regarding claim 1, Ishikawa discloses a semiconductor memory device for fast access having a timing system for controlling timing of data transfers within an semiconductor memory system, the timing system comprising: means for generating a bias signal (figure 1, timing generating circuit 112), wherein the bias signal is biased in accordance with a data address of the memory system of data being transferred (col. 6, lines 41+); and means for receiving the bias signal and generating an output clock signal, wherein the timing of the output clock signal is programmable in accordance with the bias signal (see figure 1, col. 6, lines 41+).

Regarding claim 2, Ishikawa discloses the timing system comprising all of the limitation according to claim 1, wherein the semiconductor memory is an embedded DRAM (eDRAM) memory (see figure 1).

Regarding claim 3, Ishikawa discloses the timing system comprising all of the limitation according to claim 1, wherein the bias signal is biased in accordance with the location of a memory cell corresponding to the memory address relative to a control region of the memory system (see figure 1 and its description).

Regarding claim 4, Ishikawa discloses the timing system comprising all of the limitation according to claim 1, wherein at least one of data, data address and control signal are held in a means for holding data, addresses and control signals (buffer/latch circuit to hold the signal), wherein an amount of time the at least one of data, data address and control signals are held is controlled by the output clock signal (see figure 1 and its description).

Regarding claim 5, Ishikawa discloses the timing system comprising all of the limitation according to claim 1, wherein the sum of an amount of time that the data is held in the means for holding and an amount of time that the data travels between a memory cell corresponding to the data address and the means for holding is a predetermined amount of time (see figure 1 and its description).

Regarding claim 6, Ishikawa discloses the timing system comprising all of the limitation according to claim 1, wherein a delay of the timing of the output clock signal is inversely proportional to a distance between a memory cell corresponding to the data address and the means for holding (see figure 1 and its description).

Regarding claim 7, Ishikawa discloses the timing system comprising all of the limitation according to claim 4, wherein during a first memory system clock cycle the amount of time is calculated and the at least one of data, data address and control signal are held in the means for holding, and during a subsequent second memory system clock cycle the at least one of data, data address and control signal are released from the means for holding in accordance with the amount of time and a different amount of time is calculated and a different at least one of data, data address and control signal are held in the means for holding for a subsequent data transfer (see figures 1-3 and its description).

Regarding claim 8, Ishikawa discloses the timing system comprising all of the limitation according to claim 3, wherein the data address includes first and second portions indicating the location of the memory cell relative to the control region in first and second dimensions, respectively (see figure 1 and its description).

Regarding claim 9, Ishikawa discloses the timing system comprising all of the limitation according to claim 1, wherein the means for generating the bias signal further includes a decoder circuit for decoding the data address and outputting at least one signal indicative of the data address (see figure 1).

Regarding claim 10, Ishikawa discloses the timing system comprising all of the limitation according to claim 9, wherein: the means for generating the bias signal includes at least one bias stage for receiving a respective signal of the at least one signal indicative of the data address and outputting a signal biased relative to the receive d signal; and the signal output by each bias stage of the at least one bias stage are combined to generate the bias signal (see figure 1 and its related description).

Regarding claim 11, Ishikawa discloses the timing system comprising all of the limitation according to claim 8, wherein: the means for generating the bias signal includes first and second biasing circuits; the first and second portions of the incoming data transfer address are provided to the first and second biasing circuits, respectively, for generating first and second dimension bias signals; and the means for generating the bias signal combines the first and second dimension bias signals to generate the bias signal (figures 1-2, col. 8, lines 15+).

Claims 17-20 contains the similar limitation as previously discussed in claims 1-11. Therefore, they are analyzed as previously discussed with respect to claims 1-11.

Regarding claims 21-24, the apparatus as previously discussed in claims 1-11 and 17-20 would be performed the method as claimed. Therefore, they are analyzed as previously discussed with respect to apparatus claims 1-11 and 17-20.

Allowable Subject Matter

3. Claims 12-16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

4. The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record does not show or suggest, in addition to other element in the claim, claiming the specific structure arrangement as claimed in claims 12. The means for generating the output clock signals as claimed, wherein the means for generating the output clock signal receives a pulsating clock signal and includes first and second delay stages; and wherein: the means for generating the output clock signal; the pulsating clock signal and bias signal are provided to the first delay stage for generating an intermediate clock signal having a pulse rhythm similar to the pulsating clock signal and delayed by a first delay of the timing delay; and the intermediate clock signal and the bias signal are provided to the second delay stage for generating the output clock signal having a pulse rhythm similar to the pulsating clock signal and delayed by a second delay of the timing delay.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gene N Auduong whose telephone number is (703) 305-1343.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (703) 308-4910. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

GA
April 18, 2003

Gene N Auduong
Examiner
Art Unit 2818